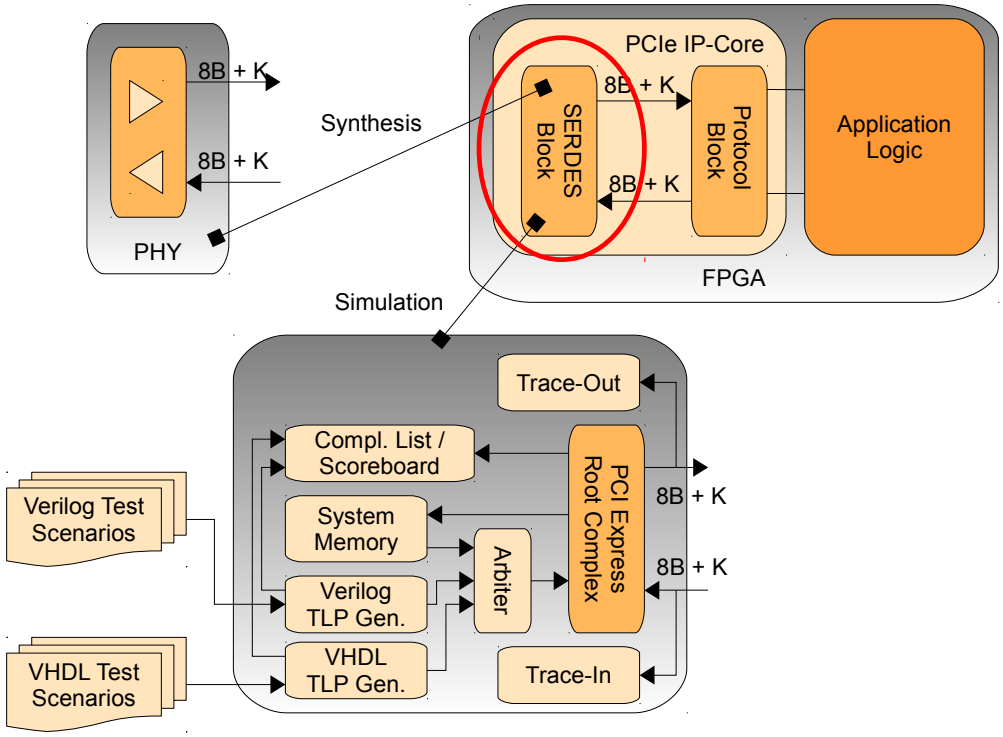
PCI Express BFM for Lattice ECPx



Introduction

Trellisys Ltd. has developed a cost-effective simulation solution for use with the Lattice PCI Express cores targeting the latters ECP2M and ECP3 FPGA families.

Lattice customers have been quick to recognise the advantages of the cost-effective PCI Express solution. The Trellisys BFM enriches this experience even further by bringing a powerful simulation vehicle to the customers finger tips.

Bus-Functional Model Description

The PCI Express bus-functional model (BFM) is designed to allow comprehensive simulation of ECP2M / ECP3 FPGAs incorporating the Lattice PCI Express cores.

The BFM provides a single engine which can be used across all ECP2M/ECP3 solutions whether configured as x1 or x4. To speed up simulation time, the BFM is a simple drop in replacement for the Lattice SERDES cell and simulates the user FPGA over the internal parallel PIPE interface.

The BFM provides method-calls for all PCI Express commands. Data payload and packet attributes (such as byte-enable settings) can be freely chosen thus allowing the user to simulate the accesses that the FPGA must really handle in the target system.

The BFM automatically performs extensive checking of PCI Express sequences such as tag-field mismatches, max. payload size monitoring and credit logic relieving the user from having to explicitly write these important checks.

All read-accesses optionally perform expected value

checking on the returned data. The BFM encompasses a dynamically sizeable memory block which models system memory. This module is used as the target for DMA access sequences generated by the user FPGA. The memory module warns the user if any location is read before being written. The user can also pre-load memory regions allowing, for example, effective simulation of user DMA scenarios in which data is read from main memory, modified and then written back.

The system memory module can also be used for communication between the test-scenario and the FPGA just as would be the case between the FPGA and the driver in the target system.

User test-scenarios can be written either in Verilog or in VHDL. Since a test-case is written in the native language (as opposed to parsing a text file), the user can continue to use the full power of the HDL language during simulation. Dynamically reactive test-scenarios are easy to write. PCI Express activity can be coordinated with other FPGA or external test-bench modules to simulate specific system corner cases.

Compiling a new test-scenario does not require re-compilation of the remaining test-bench, allowing the user to develop an effective batch-based regression methodology.

All PCI Express transactions are logged to the simulator console and marked with a time-stamp, giving the user an indication of the performance and latency to expect from the chosen solution.

System Requirements

The BFM is provided in object form for the Aldec active-hdl simulator under Windows as well as for the Aldec Riviera simulator under Windows or Linux. Minimum requirement is the mixed-language simulator version provided with the Lattice ispLever or Diamond subscription edition.

The BFM installation includes a *.pdf manual and examples in both Verilog and VHDL.

Summary

- ☑ Optimised for Aldec simulators provided with the Lattice development tools ispLever and Diamond
- ☑ Supports Verilog and VHDL
- ☑ Seamless support for PCI Express x1 and x4 configurations
- ☑ Provides advanced capabilites for simulating DMA test-scenarios
- ☑ Includes extensive error checking and transaction monitoring

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